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EXAMINER	
VLAHOS, SOPHIA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/063,316	IADANZA, JOSEPH A.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's Remarks regarding the 35 U.S.C. 103(a) rejection of independent claims 1, 8, 15, and 18 using the Cranford (U.S. 6,298,458) reference, which qualifies as prior art under 35 U.S.C. 102(e) have been considered and the rejection of claims 1, 8, 15, and 18 is withdrawn.

Therefore, the rejection and finality of the Office Action has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Schneider (U.S. 6,201,829), Drost (U.S. 6,076,175) and Ziperovich (U.S. 5,737,342).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (U.S. 6,201,829) in view of Ziperovich (U.S. 5,737,342) and Drost (U.S. 6,076,175).

With respect to claim 1, With respect to claim 1, Schneider discloses: a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network (Fig. 5, transmitter side of transceiver, elements 50, 52, 54, 40, column 4, lines 66-67, column 5, lines 1-5, column 7, lines 41-57, the 10-bit data on the self-test data bus) and for continuously generating an output signal

corresponding to the data signal; a receiver for continuously receiving the output signal from the transmitter, and for reconstructing the network data signal within the predetermined time window (Fig. 5, receiver side of transceiver, column 7, lines 58-67, column 8, lines 1-4); and a built-in-self-test (BIST) device for generating the network data signal and the control signal (Fig. 5, combination of elements 61, 62, column 8, lines 32-47) , wherein the BIST device detects erroneous performance by the transceiver based on the reconstructed network data signal (column 8, lines 48-67).

Schneider does not expressly teach: the transmitter receiving a control signal for impairing characteristics of the network data signal and for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window; and the BIST device generating the control signal and for providing a reference clock signal with a varied offset for jitter testing the transceiver.

In the same field of endeavor (testing of integrated circuits) Ziperovich discloses: a control signal for impairing characteristics of the data signal (column 9, lines 14-17, Fig. 2, bias generation block 122 and bias selection signal);

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Schneider based on the teachings of Ziperovich, so that the transmitter of Schneider receives a control signal for impairing characteristics of the network data signal and the motivation to perform such a modification is to add bias in order to test digital data processing of the chip (Ziperovich, column 4, lines 31-34). The combination of Schneider and Ziperovich discloses the limitation: and for continuously generating an output signal corresponding to the data signal and the control signal

during a predetermined time window (since phase, gain, bias is applied to the test pattern, the generated output signal corresponds to the data signal and the control signal).

In the same field of endeavor, Drost et. al., disclose: providing a reference clock signal with a varied offset for jitter testing the transceiver (column 3, lines 18-33, column 5, lines 54-67, column 6, lines 1-5, where the control signal is the variance signal).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Schneider (that teaches a BIST device) based on the teachings of Drost et. al., (i.e. providing a reference clock signal with a varied offset for jitter testing the transceiver and the motivation to perform such a modification is to determine an actual BER of chips (column 7, lines 11-20).

With respect to claim 2, all of the limitations of claim 2 are rejected above in claim 1.

With respect to claim 3, the combination of Schneider, Ziperovich, and Drost further discloses: wherein the BIST device includes a jitter control system (see the Fig. 3 of Drost. the variance circuit and variance control signal).

With respect to claim 4, all of the limitations of claim 4 are rejected above in claim 1.

4. Claims 6-7, 8-12, 15-16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (U.S. 6,201,829) in view of Ziperovich (U.S. 5,737,342), Drost (U.S. 6,076,175), and Wong (U.S. 4,754,216).

With respect to claim 6, neither Schneider, Ziperovich, Drost do not disclose: wherein the BIST device further comprises a pulse width counter for varying a pulse width of the network data signal.

In the same field of endeavor (evaluation/testing of electronic circuits) Wong discloses: a pulse width counter for varying a pulse width of the network data signal (Fig. 1, components 14, 16, 18, 20, 22 used to generate the variable pulse width data sequence, column 3, lines 38-57)

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system (BIST) of Schneider, Ziperovich, and Drost based on the teachings of Wong, in order to generate a variable pulse width network data signal using a counter for varying a pulse width of the network data signal, and the motivation behind such a modification is to test the window-time characteristics of the PLLs that are used at the transmitter and receiver (see Fig. 5 of Schneider, and column 1, lines 9-12 of Wong).

With respect to claim 7,the limitations of claim 7 are rejected above in claim 6 (Wong, the PLL tolerance window is tested, column 1, lines 21-38).

With respect to claims 8,9, claims 8, 9 are rejected based on a rationale similar to the one used to reject claims 6, 2 respectively.

With respect to claim 10, Schneider discloses: wherein the BIST device comprises means for programming the network data signal (column 5, lines 44-50, the resetable test pattern generator responds to the clock signal to generate the test patterns).

With respect to claim 11, Schneider discloses: wherein the transmitter and the receiver are provided on a single integrated circuit (column 9, line 38), the transceiver further comprising a transfer gate for selectively coupling the output signal from the transmitter to the receiver within the integrated circuit (Fig. 5, mux 55 and see column 8, lines 48-51 the mode signal supplied to the mux, gates the output signal from the transmitter to the receiver).

With respect to claim 12, Schneider discloses: wherein the network data signal includes an embedded clock signal, and wherein the BIST device comprises means for locking onto the embedded clock signal (see Fig. 5, this is the function of the RX PLL element 48).

With respect to claims 15-16 and 18-19 these claims are rejected based on a rationale similar to the one used to reject claims 8 and 12 (corresponding to both the method and program code claims).

5. Claims 13-14,17, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (U.S. 6,201,829) in view of Ziperovich (U.S. 5,737,342), Drost (U.S. 6,076,175), Wong (U.S. 4,754,216), and Ohishi et. al. (U.S. 6,087,869)

With respect to claim 13, Schneider, Ziperovich, Drost, Wong do not expressly teach: wherein the means for detecting erroneous performance by the transceiver comprises a counter device for counting edge transitions of the clock signal for establishing a time window for reconstructing the network data signal data recovered from the output signal.

Solving the same issue/problem (clock and data recovery): Ohishi et. al., disclose: a counter device for counting edge transitions of the clock signal for establishing a time window for reconstructing the network data signal data recovered from the output signal (Fig. 10, counter is part of the lock state detector of the PLL, see column 10, lines 62-67, the lock detector counts edges of the recovered clock signal, column 1, lines 31-32 the recovered clock is used to retime the data, ie. used for data receovery),

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Schneider based on the teachings of Ohishi et. al. (that teaches using a counter device for counting edge transitions of the clock signal for

establishing a time window for reconstructing the network data signal data recovered from the output signal), and the motivation to perform such a modification is to allow for the PLL to have a short lockup-time (Oishi et. al., column 6, lines 45-63 item (1) discussion of prior art problems, and column 1, lines 55-57).

With respect to claim 14, Schneider disloses: wherein the means for detecting erroneous performance by the transceiver further comprises a counter device for counting edge transitions of the network data signal within the established time window (function of signature analyzer that compares the regenerated data and the data mask pattern, see column 8, lines 60-67 and it is understood that a match/mismatch between the patterns is found when a number of matching/not matching edge data transitions is counted).

With respect to claims 17 and 20, these claims are both rejected based on a rationale similar to the one used to reject claim 13 above.

Allowable Subject Matter

6. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
5/2/2007

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